High-Speed Information Processing

UTAH STATE UNIVERSITY

CENTER

The Center for High-Speed Information Processing (CHIP) bridges the gap between university research in fast signal processing algorithms and industrial applications through software and hardware design and prototyping. CHIP's demonstrable prototypes provide companies the proof-of-concept they often require before licensing a signal processing algorithm. Applications of this technology include high definition television, hearing aids, mobile phones, image processing, space craft instrumentation, and digital receivers and transmitters.

TECHNOLOGY

CHIP's emphasis in signal processing has been the implementation of FPGA (Field Programmable Gate Array) chips. Integrated circuits (IC), or chips, function by performing many additions, subtractions, and multiplications. The Center's algorithms relieve the bottleneck in the computational speed of ICs by eliminating multipliers. This results in less power consumption, smaller chip areas, less logic gates, and faster speeds.

The multiplier-free algorithms have been implemented in the compression and restoration of hyperspectral images. These images are commonly taken by airborne or space imagers at multiple frequencies which results in noise and lost samples that need to be restored as well as very large files that need to be compressed. CHIP's fast algorithms have also been implemented in FPGA chips for the use of feedback cancellation technology in digital hearing aids as well as echo cancellation technology in telephones.

ACCOMPLISHMENTS

CHIP has been issued two patents for its echo cancellation technology and has licensed the technology to Sonic Innovations (SLC, Utah) for use in digital hearing aids and SP Communications (Logan, Utah) for use in speaker phones. The Center has also completed contract work with two other companies. In its final year, CHIP secured \$678,000 in external funding to continue its research.

